

WHAT IS CLAIMED IS:

1 1. A fractional-type phase-locked loop circuit, for synthesizing an output
2 signal multiplying a frequency of a reference signal by a selected fractional
3 conversion factor, the phase-locked loop circuit including:

4 a frequency divider for generating a feedback signal dividing the frequency of
5 the output signal by a frequency division factor selectable among at least two
6 different integer-value division factors;

7 frequency divider control means for causing the frequency division factor to
8 vary between the at least two integer-value division factors in a pre-defined number
9 of cycles, wherein an average frequency division factor over said pre-defined
10 number of cycles has a fractional value;

11 means for compensating a phase error introduced by the frequency divider on
12 the basis of a value indicative of the phase error obtained from said frequency
13 divider control means, wherein said phase-error compensation means includes
14 rounding means said rounding means receiving an input binary code with a first
15 number of binary digits, indicative of the phase error value, and providing an output
16 binary code with a second number of binary digits lower than the first number of
17 digits, the output binary code defining a rounded phase error value.

1 2. The fractional-type phase-locked loop circuit of claim 1, in which said
2 rounding means includes:

3 means for separating the input binary code into a first group of binary digits,
4 containing the less significant binary digits of the input binary code, and a second
5 group of binary digits, containing the most significant binary digits of the input binary
6 code; and

7 means for generating the output binary code by rounding a value defined by
8 the second group of binary digits according to a rounding value defined by the first
9 group of binary digits.

1 3. The fractional-type phase-locked loop circuit of claim 2, in which the
2 rounding means include an adder for adding a value defined by at least one of the
3 most significant digits of the first group of binary digits to a value defined by the
4 second group of binary digits.

1 4. The fractional-type phase-locked loop circuit of claim 2, in which the
2 rounding means further include a delta-sigma modulator receiving the first group of
3 binary digits and generating the rounding value.

1 5. The fractional-type phase-locked loop circuit of claim 1, in which the
2 phase-error-compensation means include means for generating a phase-error-
3 compensation signal from said rounded phase error value, and for using the phase-
4 error-compensation signal for conditioning a phase difference signal indicative of a
5 phase difference between the feedback signal and the reference signal.

1 6. The fractional-type phase-locked loop circuit of claim 5, in which said
2 means for generating a phase-error-compensation signal has a resolution
3 corresponding to the number of digits of the output binary code.

1 7. The fractional-type phase-locked loop circuit of claim 6, in which said
2 means for generating a phase-error-compensation signal include digital-to-analog
3 conversion means for generating the phase-error-compensation signal by converting
4 the rounded phase error value defined by the output binary code.

1 8. The fractional-type phase-locked loop circuit of claim 7, in which the
2 digital-to-analog conversion means include a multibit digital-to analog converter.

1 9. The fractional-type phase-locked loop circuit of claim 1, in which said
2 frequency divider control means include an accumulator having an accumulator
3 overflow output controlling the frequency division factor of the frequency divider, and
4 in which said input binary code carries a value contained in the accumulator.

1 10. The fractional-type phase-locked loop circuit of claim 1, in which said
2 frequency divider control means include a sigma-delta modulator for generating a
3 series of frequency divider control values determining a pattern of variation of the
4 frequency division factor of the frequency divider, said series of values being
5 generated starting from an adjustment value fed to the sigma-delta modulator, and in
6 which the phase-error compensation means includes means for generating said
7 input binary code by calculating an incremental value indicative of an incremental
8 phase error according to the conversion factor and the series of frequency divider
9 control values, and calculating the phase error value by accumulating the calculated
10 incremental value.

1 11. A circuit for compensating for a phase error between first and second
2 signals, comprising:

3 a truncator operable to receive a first data set having a first length, the first
4 data set corresponding to the phase error, the truncator further operable to modify
5 the first set to produce a second data set, the second set having a second length
6 shorter than the first length; and

7 a generator coupled to the truncator, the generator operable to generate an
8 error-compensation signal corresponding to the second set.

1 12. The circuit of claim 11 wherein the truncator comprises a separator
2 operable to separate the first set into first and second portions.

1 13. The circuit of claim 12 wherein:

2 the first portion has a third length; and

3 the truncator further comprises a modifier operable to convert the first portion
4 into a third data set having a fourth length shorter than the third length.

1 14. The circuit of claim 13 wherein the truncator further comprises a
2 combiner operable to combine the second portion with the third set.

1 15. The circuit of claim 13 wherein the modifier comprises a delta-sigma
2 modulator.

1 16. The circuit of claim 11 wherein the generator comprises a digital-to-
2 analog converter.

1 17. A circuit for compensating for a phase error between first and second
2 signals, comprising:

3 a separator operable to receive a first data set having a first length, the first
4 data set corresponding to the phase error, the separator further operable to separate
5 the first set into first and second portions, the first portion having a second length;

6 a modifier coupled to the separator, the modifier operable to convert the first
7 portion into a second data set having a third length shorter than the second length;
8 and

9 a combiner coupled to the modifier, the combiner operable to combine the
10 second portion with the second set to produce a third data set from which an error-

11 compensation signal is produced, the third set having a fourth length shorter than the
12 first length.

1 18. A method of compensating for a phase error between first and second
2 signals, comprising:

3 receiving a first data set having a first length, the first data set corresponding
4 to the phase error;

5 producing a second data set from the first set, the second set having a second
6 length shorter than the first length; and

7 producing an error-compensation signal from the second set.

1 19. The method of claim 18 wherein producing the second data set
2 comprises separating the first set into first and second portions.

1 20. The method of claim 19 wherein:

2 the first portion has a third length; and

3 producing the second data set further comprises converting the first portion
4 into a third data set having a fourth length shorter than the third length.

1 21. The method of claim 20 wherein producing the second data set further
2 comprises combining the second portion with the third set.

1 22. A phase-locked loop, comprising:

2 a circuit operable to introduce a phase error between first and second signals;

3 a truncator coupled to the circuit, the truncator operable to receive a first data
4 set having a first length, the first data set corresponding to the phase error, the

5 truncator further operable to modify the first set to produce a second data set, the
6 second set having a second length shorter than the first length; and

7 a generator coupled to the truncator, the generator operable to generate a
8 compensation signal corresponding to the second set.

1 23. An electronic system, comprising:

2 a circuit for compensating for a phase error between first and second signals,
3 comprising:

4 a truncator operable to receive a first data set having a first length, the first
5 data set corresponding to the phase error, the truncator further operable to modify

- 6 the first set to produce a second data set, the second set having a second length
- 7 shorter than the first length; and
- 8 a generator coupled to the truncator, the generator operable to generate a
- 9 compensation signal corresponding to the second set.